CHINESE OPTICS LETTERS

Vol. 20, No. 4 | April 2022

Silicon photonics integrated dynamic polarization controller

Xuyang Wang (王旭阳)[1,2*], Yanxiang Jia (贾雁翔)[1], Xubo Guo (郭旭波)[1], Jianqiang Liu (刘建强)[1], Shaofeng Wang (王少锋)[3], Wenyuan Liu (刘文元)[4], Fangyuan Sun (孙方圆)[5], Jun Zou (邹 俊)[6], and Yongmin Li (李永民)[1,2**]

[1] State Key Laboratory of Quantum Optics and Quantum Optics Devices, Institute of Opto-Electronics, Shanxi University, Taiyuan 030006, China

[2] Collaborative Innovation Center of Extreme Optics, Shanxi University, Taiyuan 030006, China

[3] College of Physics and Electronic Engineering, Shanxi University, Taiyuan 030006, China

[4] School of Science, North University of China, Taiyuan 030051, China

[5] School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore 639798, Singapore

[6] College of Science, Zhejiang University of Technology, Hangzhou 310023, China

*Corresponding author: wangxuyang@sxu.edu.cn

**Corresponding author: yongmin@sxu.edu.cn

Received September 26, 2021 | Accepted January 21, 2022 | Posted Online February 16, 2022

We designed and demonstrated experimentally a silicon photonics integrated dynamic polarization controller. The overall size of the dynamic polarization controller on chip is 2.830 mm × 0.210 mm × 1 mm. The modulation bandwidth is 30 kHz. By using a variable step simulated annealing approach, we achieve a dynamic polarization extinction ratio greater than 25 dB. A numerical simulation method was used to optimize the relevant parameters of the dynamic polarization controller. It is expected that the dynamic polarization controller can be utilized in fiber communication systems or silicon photonics integrated quantum communication systems to minimize the size and decrease the cost further.

Keywords: dynamic polarization controller; simulated annealing approach; dynamic polarization extinction ratio.
DOI: 10.3788/COL202220.041301

1. Introduction

The dynamic polarization controller (DPC) is a crucial component in fiber optic communication[1–3], optical imaging[4], and quantum technologies[5–12]. It can transform any input state of polarization (SOP) into any desired SOP to overcome polarization-related impairments, which result from high internally and externally induced birefringence. With the rapid developments in optical communication technology and large-scale optical integration technology, it is imperative to realize the traditional functions of optical polarization processing on an integration platform. In the quantum communication field, a number of research works for integrating the quantum key distribution (QKD) system on silicon photonics integrated circuits have been reported. However, a fiber DPC or manual polarization controller (MPC) was usually used instead of an on chip DPC. It is desired that the DPC can be integrated into the overall QKD chip[13–17].

Several promising platforms on integrated optic polarization controllers have been reported[18–21]. The architectures of the first two works are not based on the silicon-on-insulator (SOI) platform, which is compatible with the complementary metal-oxide-semiconductor fabrication technology that is more compact and economical. The design in Ref. [20] has several functions; however, arbitrary polarization-based coordinate conversion cannot be performed because no symmetrical 2D grating is used to couple the light out from the chip. The design in Ref. [21] cannot realize the endless polarization control. Especially, the DPC based on the simulated annealing method was not explored, and the results of the dynamic extinction ratio were not investigated.

In this work, we design and demonstrate a full silicon photonics integrated DPC. By employing the variable step simulated annealing approach, we achieve a dynamic polarization extinction ratio greater than 25 dB. The experimental results agree well with theoretical simulation. The performance of the compact silicon photonics integrated polarization controller is close to that of the commercial fiber DPC. The overall size of the DPC on chip was 2.830 mm × 0.210 mm × 1 mm, which was much smaller than that of fiber-squeezers-based DPC.

In Section 2, the design of the silicon photonics integrated DPC is presented. In Section 3, the characters of the thermal phase shifters (TPSs) are evaluated. There is good linearity between the phase shift and the power consumed by the metal

heater. The modulation bandwidth is about 30 kHz. In Section 4, we present the numerical simulation and experimental results of the silicon photonics integrated DPC. The advantages of the variable step simulated annealing approach are demonstrated, and a dynamic polarization extinction ratio larger than 25 dB is obtained. Finally, Section 5 presents the ways to improve the performance of the DPC and the conclusions.

2. Design of Silicon Photonics Integrated DPC

Generally, the DPC comprising three or four fiber squeezers was utilized in fiber communication systems. The fiber squeezers were activated by piezoceramic actuators, which were driven by the high voltage of above 100 V. The squeezers alternated between 0°, 45°, 0°, and 45° of orientation. Each squeezer introduced a phase shift between the linear polarization components aligned parallel and perpendicular to the squeezing direction. The phase shift can be varied by altering the squeezing force. The fiber under the stress can be represented in Jones calculus by two kinds of transformation matrices M_0 and M_{45}, as indicated in Eq. (1):

$$M_0 = \begin{pmatrix} e^{-i\delta_0/2} & 0 \\ 0 & e^{i\delta_0/2} \end{pmatrix}, \quad M_{45} = \begin{pmatrix} \cos(\delta_{45}/2) & -i\sin(\delta_{45}/2) \\ -i\sin(\delta_{45}/2) & \cos(\delta_{45}/2) \end{pmatrix}, \tag{1}$$

where δ_0 and δ_{45} are the delayed phases due to stressed fiber birefringence. The matrix M_{45} can be transformed to a product of matrix M_0 and matrices, which describe 50/50 couplers, as follows:

$$M_{45} = \begin{pmatrix} \cos(\delta_{45}/2) & -i\sin(\delta_{45}/2) \\ -i\sin(\delta_{45}/2) & \cos(\delta_{45}/2) \end{pmatrix} = \begin{pmatrix} 1/\sqrt{2} & -1/\sqrt{2} \\ 1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix} \begin{pmatrix} e^{-i\delta_{45}/2} & 0 \\ 0 & e^{i\delta_{45}/2} \end{pmatrix} \begin{pmatrix} 1/\sqrt{2} & 1/\sqrt{2} \\ -1/\sqrt{2} & 1/\sqrt{2} \end{pmatrix}. \tag{2}$$

The transformation matrices can be transformed into the corresponding structures of silicon photonics integrated circuits, as demonstrated in Fig. 1[22]. The blue lines denote the waveguides. The red and black rounded rectangles denote the TPSs and 50/50 multimode interferometers (MMIs), respectively.

According to the above basic structures, the DPC consisting of silicon photonics integrated circuits was designed, as indicated in Fig. 2(a). The input and output ports were 2D grating couplers (GCs) that were utilized as the polarization beam splitter (PBS)[23]. The structure was symmetrical, the input port can be utilized as an output port, and vice versa. Four 1×2 50/50 MMI couplers were inserted into the waveguides for the purpose of testing and aligning, where one output port of each 1×2 MMI coupler is connected to a one-dimensional (1D) GC or a photodiode. The 1550 nm laser beam in single-mode (SM) fiber with an arbitrary SOP can be guided into the integrated DPC by a vertical coupling approach. Each linear polarization component is directed into one waveguide with TE mode using the 2D GC. Following a series of transformations, such as $M_1(M_0)$, $M_2(M_{45})$, $M_3(M_0)$, and $M_4(M_{45})$, the two TE modes of each waveguide are coupled out to another SM fiber through the 2D GC.

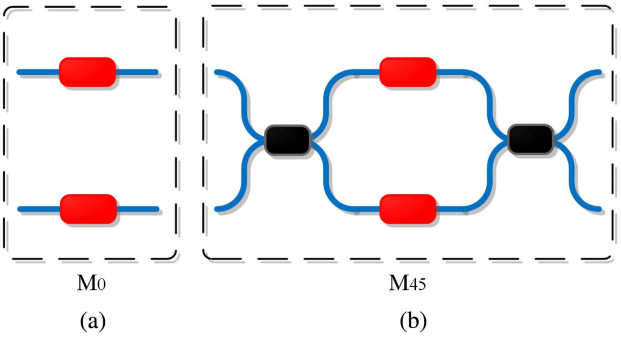

Fig. 1. Structures of silicon photonics integrated circuits corresponding to the transformation matrices M_0 and M_{45}. (a) The structure corresponds to matrix M_0; (b) the structure corresponds to matrix M_{45}.

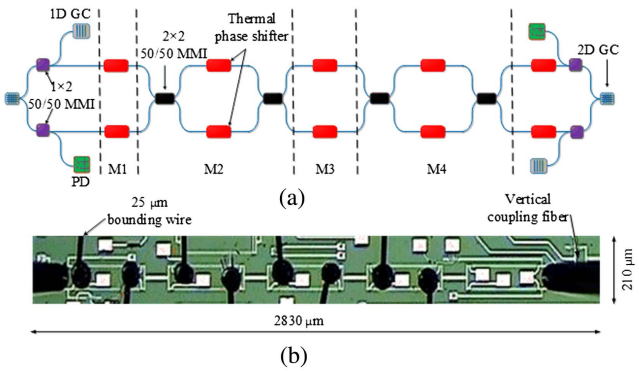

Fig. 2. Structure and photograph of silicon photonics integrated DPC. PD, photodiode. (a) The structure of the DPC; (b) the photograph of the DPC.

Figure 2(b) indicates the photograph of silicon photonics integrated DPC. The fabrication of the device was performed with CSiP180Al active flow technology. It was based on a 200 mm SOI substrate with 2 μm buried oxide (BOX) and 220 nm top silicon. The overall size of the DPC was 2.830 mm × 0.210 mm × 1 mm, which was much smaller than that of the fiber-squeezers-based DPC with the size of 83 mm × 20.32 mm × 16 mm (PolaRITE III, GP). Here, TPS was employed to alter the delayed phase. The 25 μm golden wire was selected to bond the pad by which the driving voltage can be applied on the DPC. The characters of the TPS are evaluated in detail in the next section.

3. Characterization of the TPS

The characters of the TPS or TiN metal heater are evaluated utilizing a Mach–Zehnder (MZ) modulator. The length of the TPS

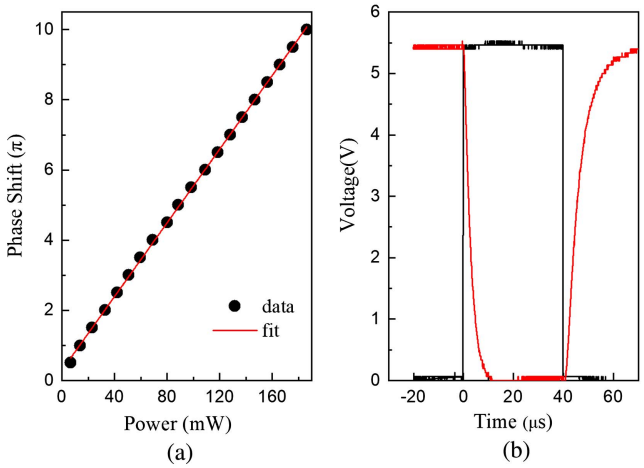

Fig. 3. Characterization of the TPS. (a) The phase shift versus the consumed power of the thermal heater; (b) the rise and fall time of the MZ modulator.

is 400 μm, and the resistance of the metal heater is 1.97 kΩ. A 1 mW 1550 nm continuous laser beam was coupled into one port of the 2 × 2 MZ modulator. By varying the voltage on the metal heater of one side, the output power was altered. We transformed the voltage into the power applied on the metal heater utilizing the expression

$$P = V^2/R, \tag{3}$$

where R denotes the resistance of the metal heater.

As shown in Fig. 3(a), there is a good linearity between the phase shift and the power consumed by the metal heater. The total phase shift is roughly 3π by varying the power from 0 to 50.56 mW, which corresponds to the applied voltage from 0 to 10 V. The phase shift amount is enough to stabilize the polarization with the simulated annealing method. Note that many digital-to-analog converter chips' output voltages can reach this voltage, and a high voltage amplifier is unnecessary. In contrast, the voltage of 140 V is required to drive the piezo of PolaRITE III.

In addition, the modulation speed of the phase was evaluated, which determines the polarization locking speed. In the measurement, a 40 μs electronic square pulse with a peak voltage of 5.6 V was applied to the metal heater of the MZ modulator. It corresponds to a phase shift of π. The rising time was measured to be 11 μs, and the falling time is 5.9 μs. This value is about one-tenth of the rise time of PolaRITE III. Thus, the modulation bandwidth is about 30 kHz.

4. Numerical Simulation and Experimental Results

The simulated annealing approach is a good approach to lock the output SOP. Usually, a big step is needed to realize high-speed polarization controlling. However, from the simulation, we discovered that to obtain a higher polarization extinction ratio, a small step is necessary. To address this issue, the variable

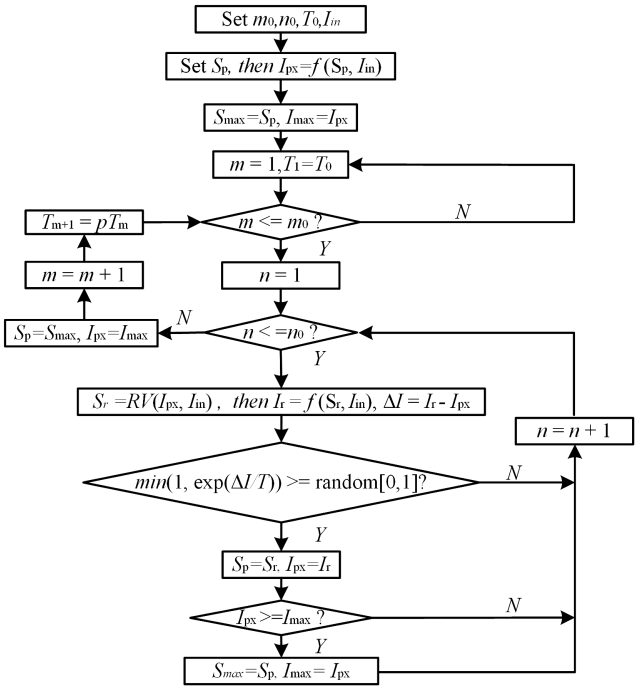

Fig. 4. Flow chart of the variable step simulated annealing method.

step approach was adopted to increase the speed and extinction ratio of the SOP locking simultaneously. The flow chart of the program is illustrated in Fig. 4.

We started by setting the initial temperature as $T_0 = 1$ K. The variable m is used to count the external loops, and the number of the total loops is $m_0 = 10$ in a round. The variable n is used to count the internal loops, and the number of the total loops is $n_0 = 50$ in an external loop. There are totally 500 internal loops in a round. The maximal intensity of the input beam I_{in} is normalized. Then, we set the initial value of the four delay phases to 2π and stored them into an array $S_p(\theta_1,\theta_2,\theta_3,\theta_4)$. Then, we calculated the output intensity I_{px} according to the delay phases and the SOP of the input beam. Here, I_{px} denotes the intensity of the beam from one output port of the PBS followings the DPC. I_{max} and S_{max} denote the maximum intensity of I_{px} and corresponding delayed phases, respectively. I_{py} denotes the intensity of the beam from the other output port of the PBS.

Before entering the external loop, the value m was initialized to one, and the value T_1 was initialized to T_0. In the external loop, the temperature decreases with the proportion function:

$$T_{n+1} = pT_n, \tag{4}$$

where the value of p is set to 0.2. It determines the temperature changing speed. When entering the internal loop, we employed the random variable step function RV(I_{px},I_{in}) to generate random phase delay S_r. The random variable step function is expressed as follows:

$$S_r = \begin{cases} S_p + \mathrm{st} \cdot r, & S_p \le 0 \\ S_p + c \cdot \mathrm{st} \cdot r, & 0 < S_p < 3\pi \\ S_p - \mathrm{st} \cdot r, & 3\pi \le S_p \end{cases}, \tag{5}$$

where r denotes the random numbers between 0 and 1, c denotes the random numbers of -1 or 1, and st represents the search step. Usually, when the step st is larger, the search loops are less. However, the disturbance generated by the large step st is also higher, making a high extinction ratio of SOP difficult to obtain. We proposed to use a variable step st to improve the extinction ratio and, at the same time, to maintain a high search speed. The variable steps are indicated by

$$\mathrm{st} = \begin{cases} 0.16\ \mathrm{rad}, & 0.1 < I_{\mathrm{st}} \le 1 \\ 0.08\ \mathrm{rad}, & 0.01 < I_{\mathrm{st}} \le 0.1 \\ 0.03\ \mathrm{rad}, & 0.001 < I_{\mathrm{st}} \le 0.01 \\ 0.008\ \mathrm{rad}, & I_{\mathrm{st}} \le 0.001 \end{cases}, \tag{6}$$

where $I_{\mathrm{st}} = 1 - I_{px}$ defines the gap between the normalized maximum intensity 1 and I_{px}.

The simulation results are shown in Fig. 5. The fixed step method with two different steps and the variable step method were compared. When the step was larger (st = 0.16 rad), the required internal loops were less. However, the extinction ratio is lower. For a smaller step of st = 0.008 rad, a higher extinction ratio can be obtained at the cost of more internal loops to reach the steady value. It is obvious that the best result is achieved by the variable step simulated annealing methods, where the highest extinction ratio is obtained with the least internal loops.

Note that the static polarization extinction ratio, electronic noises of the photodetectors, and fluctuations of the optical power determine the ultimate limit of the DPC. In the simulation, the minimum intensity of I_{py} is set to $I_{px} \cdot 10^{-2.8}$, considering the statistic polarization extinction ratio of the 2D GC of 28 dB. The standard variance of the electronic noises and optical

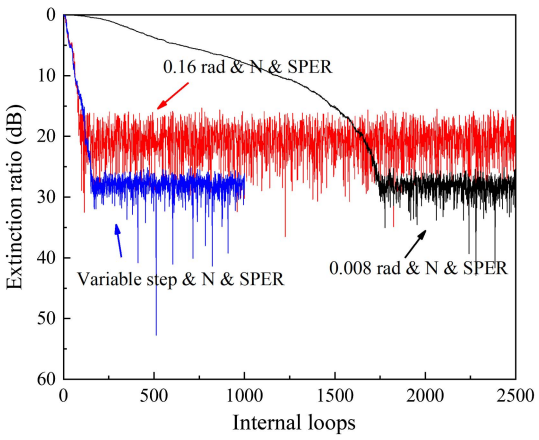

Fig. 5. Simulation results of dynamic polarization control. It represents the extinction ratio versus the number of the internal loops with fixed and variable step simulated annealing methods. The noise and static polarization extinction ratio were considered. N, noise; SPER, static polarization extinction ratio.

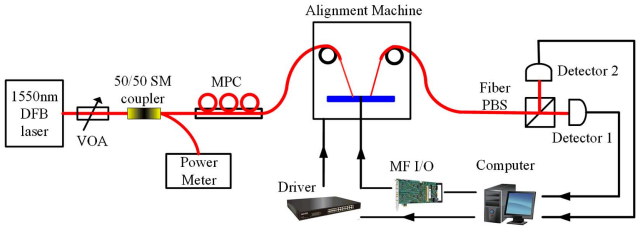

Fig. 6. Experimental setup to test the silicon photonics integrated DPC. MPC, manual polarization controller; MF, multifunctional.

power fluctuation is set to 5×10^{-4} (normalized to the maximum intensity of one).

The scheme of the test setup is illustrated in Fig. 6. A 1550 nm fiber pigtailed DFB laser was utilized to generate a continuous beam, and a variable optical attenuator is used to tune the intensity of the laser beam. Part of the beam, which was employed to monitor the laser power, was separated by a 50/50 fiber SM coupler. An MPC is employed to tune the SOP of the beam directed into the chip. An alignment machine was utilized to align the fiber to the top of the 2D GC nearly vertically with an angle of 80°. The power coupled into the chip is 1 mW. The measured total loss from the input 2D GC to the output 2D GC is ~20 dB. The coupling loss of the fabricated 2D GC is 7 dB. Considering the 3 dB loss from the 50/50 MMI on the chip, the transmission loss of the integrated DPC is 3 dB, which mainly originates from the four MMIs. After transmitting through the chip, the beam was directed into the SM fiber again. Then, it was separated by the fiber PBS into path 1 and path 2. The intensity of the beam in the paths was evaluated by detector 1 and detector 2. The DPC on the chip is exploited to maximize the intensity of the beam in path 1 (detector 1), and, therefore, the intensity of the beam in path 2 (detector 2) is minimized.

Based on the simulation results, we employed the variable step approach to lock the SOP of the laser. The output voltage limit of the multifunction input/output (I/O) card was 10 V. From Section 3, this voltage range can result in a phase shift of 3π. This phase shift range is enough to lock the SOP by setting the initial phase shift at 2π. By fitting the experiment results in Fig. 3(a), a linear formula can be obtained as follows:

$$\theta = c \cdot P + \theta_{\mathrm{bias}}, \tag{7}$$

where $c = 164.85\ \mathrm{rad/mW}$, and $\theta_{\mathrm{bias}} = 0.93$ rad. Combined with Eq. (3), the relationship between the voltage step ΔV and corresponding phase step $\Delta\theta$ can be written as

$$\Delta V = \frac{R}{2cV}\Delta\theta. \tag{8}$$

From Eq. (8), we observe that ΔV decreases with the voltage V for a constant $\Delta\theta$. When the value of voltage V is small, the voltage step ΔV will be very large. The minimum value ΔV_{min} corresponds to the maximum value of V_{max}, and it is not relevant to θ_{bias}. In our experiment, ΔV_{min} was used to ensure more stable polarization control for the corresponding $\Delta\theta$ or st value.

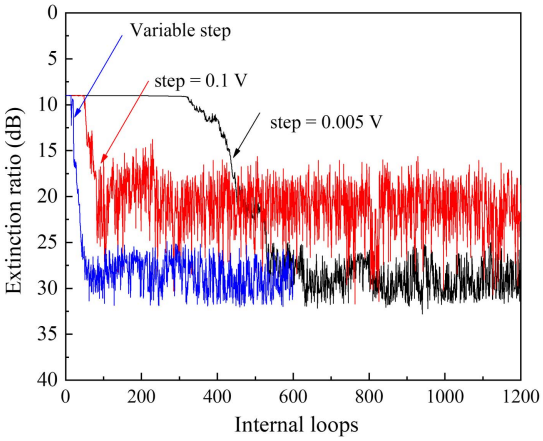

Fig. 7. Experiment results of dynamic polarization control. It represents the extinction ratio versus the number of internal loops with fixed and variable step simulated annealing methods.

The experiment results of our silicon photonics integrated dynamic polarization controlling are shown in Fig. 7. Before the operation of the DPC control procedure, the voltage of detector 2 was set to the maximum value by the MPC. For the measurement range of detector 2, its output was saturated at the beginning of the DPC control. The black line represents the results utilizing a fixed step of 0.005 V (0.008 rad at $V = 10$ V) with ~600 internal loops. The red line represents the results utilizing a fixed step of 0.1 V (0.16 rad at $V = 10$ V) with ~100 internal loops. The blue line represents the results utilizing a variable step. For the variable step approach, a extinction ratio higher than 25 dB is obtained with ~100 internal loops. This value is nearly close to the static extinction ratio of 28 dB of our silicon photonics integrated DPC. The experimental results are similar to the simulation results in Fig. 5. To achieve a better dynamic polarization extinction ratio in experiment, a low noise photodetector should be utilized, and multiple samples were averaged to minimize the electronic noise and optical power fluctuation.

5. Discussion and Conclusions

For further study, it is very promising to decrease the coupling efficiency of the silicon photonics integrated DPC from 7 dB to 2 dB or less by using the butting coupling method with an appropriate spot size converter between the on-chip silicon waveguide and SM fiber. On the SM fiber side, a fiber lens or large numerical aperture optical fiber is recommended. On the integrated DPC side, the spot size converter and polarization rotator-splitter should be used to replace the 2D GC[24]. In consideration of deleting the unnecessary 1×2 MMI coupler, the total insertion loss can be reduced to about 6.8 dB. In the situations of less reset, the structure of the DPC can be simplified from 0°, 45°, 0°, 45° to 0°, 45°, 0°. Then, the total insertion loss will be reduced to about 5.4 dB.

The modulation bandwidth of the DPC designed by us is about 30 kHz. Considering the voltage of 5.6 V applied on the TPS, the bandwidth-voltage product is $5.6 \times 30 = 168$ kHz · V. Therefore, the bandwidth-voltage product is much higher than the commercial product based on squeezing the fiber (PolaRITE III with driving board PCD - M02), which has a typical value of 1.25 kHz·V. More importantly, the high voltage about 140 V is no longer needed. Considering that a faster modulation speed is needed in some cases, the P-I-N phase shifter based on the plasma dispersion effect of silicon can be used to replace the TPS. The modulation bandwidth of tens of MHz or higher can be achieved. However, the insertion loss of the P-I-N phase shifter is higher, and the loss increases with the phase shift amount. This will affect the balance of the two arms and decrease the polarization extinction ratio of the DPC. Typically, for a 500 μm long P-I-N phase shifter, the insertion loss is about 0.5–1 dB or even smaller. The excess insertion loss is 0.1–0.2 dB when the phase shift amount is π, and the excess insertion loss is 0.5–1 dB when the phase shift amount is 3π.

Compared with the polarization controllers based on silicon photonics integrated circuits[20,21], our DPC utilizes an output 2D GC and 0°/45°/0°/45° structure, which makes it able to realize arbitrary polarization-based coordinate conversion with endless polarization control.

In conclusion, we have designed and demonstrated a compact silicon photonics integrated DPC. The structures and principles of operation were presented in detail. A polarization extinction ratio higher than 25 dB was achieved with the variable step simulated annealing approach. Numerical simulation was used to optimize the experimental parameters. The methods to decrease the loss and increase the modulation speed for the device are also discussed. With the butting coupling method and polarization rotator-splitter, the effective transmission loss will be significantly reduced, resulting in a better transmission performance of fiber communication systems. It is expected that the device can also find applications in silicon photonics integrated QKD systems.

Acknowledgement

This work was supported by the Aeronautical Science Foundation of China (No. 20200020115001), National Natural Science Foundation of China (No. 62175138), Key Research and Development Program of Guangdong Province (No. 2020B0303040002), Shanxi 1331KSC, and Open Project of the State Key Laboratory of Quantum Optics and Quantum Optics Devices of Shanxi University (No. KF202006).

References

1. D. X. Dai, C. L. Li, S. P. Wang, H. Wu, Y. C. Shi, Z. H. Wu, S. M. Gao, T. G. Dai, H. Yu, and H. K. Tsang, "10-channel mode (de)multiplexer with dual polarizations," Laser Photon Rev. **12**, 1700109 (2018).
2. J. Wang, S. L. He, and D. X. Dai, "10-channel mode (de)multiplexer with dual polarizations," Laser Photon Rev. **8**, L18 (2018).

3. Z. Y. Chen, L. S. Yan, Y. Pan, L. Jiang, A. L. Yi, W. Pan, and B. Luo, "Use of polarization freedom beyond polarization-division multiplexing to support high-speed and spectral-efficient data transmission," Light Sci. Appl. **6**, e16207 (2017).
4. J. S. Tyo, D. L. Goldstein, D. B. Chenault, and J. A. Shaw,"Review of passive imaging polarimetry for remote sensing applications," Appl. Opt. **45**, 5453 (2006).
5. D. S. Ding, W. Zhang, Z. Y. Zhou, S. Shi, B.-S. Shi, and G. C. Guo, "Raman quantum memory of photonic polarized entanglement," Nat. Photonics **9**, 332 (2015).
6. P. Jouguet, S. Kunz-Jacques, A. Leverrier, P. Grangier, and E. Diamanti, "Experimental demonstration of long-distance continuous-variable quantum key distribution," Nat. Photonics **7**, 378 (2013).
7. J. W. Wang, F. Sciarrino, A. Laing, and M. G. Thompson, "Integrated photonic quantum technologies," Nat. Photonics **14**, 273 (2020).
8. X. Y. Wang, W. Y. Liu, P. Wang, and Y. M. Li, "Experimental study on all-fiber-based unidimensional continuous-variable quantum key distribution," Phys. Rev. A **95**, 062330 (2017).
9. Y. C. Zhang, Z. Y. Chen, S. Pirandola, X. Y. Wang, C. Zhou, B. J. Chu, Y. J. Zhao, B. J. Xu, S. Yu, and H. Guo, "Long-distance continuous-variable quantum key distribution over 202.81 km of fiber," Phys. Rev. Lett. **125**, 010502 (2020).
10. E. Diamanti, H. K. Lo, B. Qi, and Z. Yuan, "Practical challenges in quantum key distribution," NPJ Quant. Inf. **2**, 16025 (2016).
11. G. F. Xin, L. Shen, H. Y. Pi, D. J. Chen, H. W. Cai, H. Z. Feng, J. X. Geng, R. H. Qu, G. T. Chen, Z. J. Fang, and W. B. Chen, "Polarization-locked VCSEL with PM fiber pigtail for quantum communication," Chin. Opt. Lett. **10**, 101403 (2012).
12. P. Y. Zhang, L. L. Lu, F. C. Qu, X. H. Jiang, X. D. Zheng, Y. Q. Lu, S. N. Zhu, and X. S. Ma, "High-quality quantum process tomography of time-bin qubit's transmission over a metropolitan fiber network and its application," Chin. Opt. Lett. **18**, 082701 (2020).
13. K. Wei, W. Li, H. Tan, Y. Li, H. Min, W. J. Zhang, H. Li, L. X. You, Z. Wang, X. Jiang, T. Y. Chen, S. K. Liao, C. Z. Peng, F. H. Xu, and J. W. Pan, "High-speed measurement-device-independent quantum key distribution with integrated silicon photonics," Phys. Rev. X **10**, 031030 (2020).
14. C. X. Ma, W. D. Sacher, Z. Y. Tang, J. C. Mikkelsen, Y. Yang, F. H. Xu, T. Thiessen, H. K. Lo, and J. K. S. Poon, "Silicon photonic transmitter for polarization-encoded quantum key distribution," Optica **3**, 1274 (2020).
15. P. Sibson, J. E. Kennard, S. Stanisic, C. Erven, J. L. O'Brien, and M. G. Thompson, "Integrated silicon photonics for high-speed quantum key distribution," Optica **4**, 172 (2017).
16. P. Sibson, C. Erven, M. Godfrey, S. Miki, T. Yamashita, M. Fujiwara, M. Sasaki, H. Terai, M. G. Tanner, C. M. Natarajan, R. H. Hadfield, J. L. O'Brien, and M. G. Thompson, "Chip-based quantum key distribution," Nat. Commun. **8**, 13984 (2017).
17. G. Zhang, J. Y. Haw, H. Cai, F. Xu, S. M. Assad, J. F. Fitzsimons, X. Zhou, Y. Zhang, S. Yu, J. Wu, W. Ser, L. C. Kwek, and A. Q. Liu, "An integrated silicon photonic chip platform for continuous-variable quantum key distribution," Nat. Photonics **13**, 839 (2019).
18. J. D. Sarmiento-Merenguel, R. Halir, X. Le Roux, C. Alonso-Ramos, L. Vivien, P. Cheben, E. Durán-Valdeiglesias, I. Molina-Fernández, D. Marris-Morini, D. X. Xu, and J. H. Schmid, "Demonstration of integrated polarization control with a 40 dB range in extinction ratio," Optica **2**, 1019 (2015).
19. J. W. Kim, S. H. Park, W. S. Chu, and M. C. Oh, "Integrated-optic polarization controllers incorporating polymer waveguide birefringence modulators," Opt. Express **20**, 12443 (2012).
20. H. L. Zhou, Y. H. Zhao, Y. X. Wei, F. Li, J. J. Dong, and X. L. Zhang, "All-in-one silicon photonic polarization processor," Nano Photonics **8**, 2257 (2019).
21. P. Velha, V. Sorianello, M. V. Preite, G. De Angelis, T. Cassese, A. Bianchi, F. Testa, and M. Romagnoli, "Wide-band polarization controller for Si photonic integrated circuits," Opt. Lett. **41**, 5656 (2016).
22. L. Moller, "WDM polarization controller in PLC technology," IEEE Photon. Technol. Lett. **13**, 585 (2001).
23. J. Zou, Y. Yu, and X. L. Zhang, "Two-dimensional grating coupler with a low polarization dependent loss of 0.25 dB covering the C-band," Opt. Lett. **41**, 4206 (2016).
24. J. Zou, X. Ma, X. Xia, C. H. Wang, M. Zhang, J. H. Hu, X. Y. Wang, and J. J. He, "Novel wavelength multiplexer using $(N+1)\times(N+1)$ arrayed waveguide grating and polarization-combiner-rotator on SOI platform," J. Lightwave Technol. **39**, 2431 (2021).